CLAIMS:

1. A semiconductor CMOS processing method of forming NMOS and PMOS circuitry comprising exposing desired PMOS regions over a substrate into which p-type impurity is to be provided while contemporaneously forming a contact opening to at least one conductive line extending over isolation oxide.

2. The CMOS processing method of claim 1 further comprising prior to the exposing forming at least one nitride containing insulative cap over the at least one conductive line.

3. The CMOS processing method of claim 1 further comprising prior to the exposing forming an insulative cap over the at least one conductive line, the insulating cap comprising a nitride layer and an oxide layer thereatop.

4. The CMOS processing method of claim 1 further comprising:

prior to the exposing, forming an insulative cap over the at least one conductive line, the insulating cap comprising a nitride layer and an oxide layer thereatop, the step of forming the contact opening leaving behind at least some of the nitride layer; and

after the exposing, providing p-type impurity into the exposed PMOS regions to form desired source/drain regions.

5. The CMOS processing method of claim 1, wherein the exposing and the forming are accomplished using at least two etches.

6. The CMOS processing method of claim 1, wherein the exposing and forming are accomplished using a wet etch and a dry etch.

7. The CMOS processing method of claim 1, wherein the exposing and forming are accomplished using at least two etches, a first of which comprises a dry etch.

8. A semiconductor processing method comprising in a common masking step, forming a contact opening to a conductive line over a substrate and forming an opening to a laterally spaced substrate active area.

9. The CMOS processing method of claim 8, wherein the conductive line includes a nitride containing cap a portion of which is removed during formation of the contact opening.

10. The CMOS processing method of claim 8 further comprising:

prior to the forming steps, forming a photoresist layer over the substrate and patterning the photoresist layer with a desired contact opening and an opening to a laterally spaced substrate active area, wherein the steps of forming a contact opening and an opening to the laterally spaced substrate active area comprise anisotropically etching a protective material over the conductive line to define the contact opening with a desired lateral width dimension, the etch also defining a doping window through which impurity is to be provided to the substrate active area, the doping window having a lateral width dimension which is greater than the lateral width dimension of the contact opening; and

after the etching step, angle doping the substrate with a p-type impurity to form at least one source/drain region in the active area.

11. A semiconductor CMOS processing method of forming PMOS source/drain regions over a substrate comprising doping desired PMOS source/drain regions in the absence of any photoresist over NMOS regions of the substrate.

12. The CMOS processing method of claim 11 wherein the doping step is carried out by ion implantation.

13. The CMOS processing method of claim 11 wherein the doping step is carried out by gas chemical diffusion.

14. The CMOS processing method of claim 11 further comprising prior to the doping step:

forming an oxide layer over the substrate; and

in a common masking step, patterning: a) a contact opening to a conductive line extending over isolation oxide and, b) a doping window to a substrate active area which is to retain the PMOS source/drain regions.

15. A semiconductor CMOS processing method of forming NMOS source/drain regions over a substrate comprising doping desired NMOS source/drain regions in the absence of any photoresist over PMOS regions of the substrate.

16. A semiconductor CMOS processing method comprising, in the same processing steps, exposing PMOS active areas on a substrate into which p-type impurity is to be provided and forming contact openings to substrate gate lines.

17. The CMOS processing method of claim 16, wherein the gate lines include a protective cap at least a portion of which contains a nitride material and the forming step comprises removing at least some of the protective cap.

18. The CMOS processing method of claim 16, wherein the gate lines include a protective cap at least a portion of which contains a nitride material with an oxide material elevationally outward thereof, and the forming step comprises removing at least some of the protective cap.

19. The CMOS processing method of claim 16 further comprising after the exposing and forming steps, gas diffusion doping the exposed PMOS active areas to form source/drain regions.

20. A semiconductor processing method of forming a contact opening to a conductive gate line which overlies a substrate active area and substrate isolation area comprising, in a common masking step, patterning and etching a contact opening to a portion of the conductive gate line which overlies the substrate isolation area, the patterning and etching also outwardly exposing substrate active area to accommodate source/drain doping adjacent the gate line in the substrate active area.

21. The semiconductor processing method of claim 20, wherein the conductive gate line includes a nitride containing cap a portion of which is removed during formation of the contact opening.

22. The semiconductor processing method of claim 20, wherein the conductive line includes a nitride containing cap with an upper oxide portion which is removed during formation of the contact opening to expose at least some of the nitride containing portion.

23. The semiconductor processing method of claim 20, wherein the etching defines a doping window through which the desired substrate active area is exposed, the doping window having a greater lateral width dimension than the contact opening.

24. The semiconductor processing method of claim 20, wherein the etching defines a doping window through which the desired substrate active area is exposed, the doping window having a greater lateral width dimension than the contact opening and further comprising angle doping the exposed substrate active area to form source/drain regions.

25. A semiconductor CMOS processing method comprising:

forming a doping window over a PMOS active area on a substrate, the doping window having a first open lateral width;

forming a contact opening over a conductive line, the contact opening having a second open lateral width which is less than the first open lateral width; and

after forming the doping window and contact opening, subjecting the substrate to angled ion implant doping of p-type material to form PMOS source/drain regions in the PMOS active area.

26. The CMOS processing method of claim 25, wherein forming the doping window and a contact opening are accomplished in a common masking step.

27. The CMOS processing method of claim 25, wherein the conductive line comprises a polysilicon layer, a silicide layer atop the polysilicon layer, and a protective capping layer atop the silicide layer, the protective capping layer comprising at least one nitride layer and an oxide layer atop the at least one nitride layer.

28. A semiconductor processing method of forming PMOS circuitry having PMOS source/drain regions over a semiconductor substrate comprising:

exposing desired PMOS source/drain active areas over the substrate;

providing p-type impurity to a first concentration into the exposed PMOS source/drain active areas;

forming a masking layer over the substrate;

patterning and etching the masking layer to form openings over the PMOS source/drain active areas; and

providing p-type impurity through the openings into the PMOS source/drain active areas to a second concentration which is greater than the first concentration.

29. The semiconductor processing method of claim 28 further comprising forming NMOS circuitry over the substrate, the PMOS circuitry and the NMOS circuitry collectively defining CMOS circuitry.

30. The semiconductor processing method of claim 28, wherein the openings are smaller in cross section than the source/drain regions.

31. The semiconductor processing method of claim 28, wherein the patterning and etching comprises forming at least one contact opening to a conductive line formed over the substrate.

32. A semiconductor processing method of forming a contact opening to a conductive word line which overlies a substrate active area comprising:

forming a conductive word line over a substrate, a portion of the word line overlying a field isolation region and extending laterally away therefrom and over a substrate active area;

encapsulating the word line with nitride encapsulating material;

forming an oxide layer over the substrate, the oxide layer covering the conductive word line and the substrate active area; and

in a common step, patterning and etching the oxide layer to outwardly expose at least one desired substrate active area into which p-type impurity is to be provided, the etching also forming a contact opening over that portion of the conductive word line overlying the field isolation region.

33. The semiconductor processing method of claim 32, wherein the etching step etches the oxide material at substantially the same rate as the nitride encapsulating material.

34. A semiconductor processing method comprising:

forming at least one conductive gate line over a substrate, the gate line including a silicide layer, the gate line overlying a field isolation region and extending laterally away therefrom and over substrate active area;

providing a nitride material over the silicide layer;

forming an oxide layer over the at least one conductive line and the substrate active area; and

conducting an anisotropic etch to a degree sufficient to: (a) remove at least some of the nitride material over the conductive line to define a contact opening thereto and, (b) remove enough of the oxide layer over the substrate active area to expose source/drain regions into which p-type impurity is to be added.

35. The semiconductor processing method of claim 34, wherein the nitride material and the oxide layer are etched at substantially the same rate.

36. The semiconductor processing method of claim 34 further comprising gas diffusion doping the exposed source/drain regions with a p-type impurity.

37. A semiconductor processing method of forming a contact opening to a conductive line comprising:

forming a conductive line over a substrate, the conductive line having a conductive portion and a protective portion over the conductive portion, the protective portion comprising at least a nitride layer atop the conductive line and an oxide layer atop the nitride layer, at least a part of the conductive line extending over a substrate active area;

forming nitride encapsulation material over the conductive line and its protective portion; and

in a common masking step, etching a doping window opening over the substrate active area adjacent the line and removing at least some of the nitride encapsulation material and some of the protective portion of the conductive line to form a contact opening to the conductive line.

38. A semiconductor method of forming a conductive line comprising:

forming a conductive gate stack atop a substrate;

forming a nitride layer atop the gate stack;

forming an oxide layer atop the nitride layer;

forming nitride encapsulation material over the oxide layer, the nitride layer and the conductive gate stack;

selectively removing at least some of the nitride encapsulation material relative to the oxide layer; and

selectively removing at least some of the oxide layer relative to the nitride layer, the removing steps defining at least part of a contact opening over the gate stack.

39. A semiconductor CMOS processing method of forming CMOS circuitry comprising:

forming a substrate comprising a plurality of layers;

etching at least some of the plurality of layers to form at least one conductive gate line, the at least one gate line overlying a field isolation region and having a conductive line top;

forming a nitride material over at least a portion of the conductive gate line top;

forming an oxide layer over the nitride material;

planarizing the oxide layer;

forming a photoresist layer over the planarized oxide layer;

in a common masking step, patterning the photoresist layer to form a contact opening over the conductive gate line and a doping window over active area of the substrate adjacent the gate line, the contact opening and the doping window having respective lateral width dimensions, the contact opening width dimension being less than the doping window width dimension;

anisotropically etching both the nitride material and the oxide layer at substantially the same rate to respectively define a contact opening to the conductive gate line and a doping window over the substrate active area adjacent the gate line; and

doping desired areas of the substrate active area with a p-type impurity to form at least a portion of *one source/drain region.